

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/2000
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventors: Pak Shing Chau, et al.
	Group Art Unit: Unknown
"LOW-LATENCY EQUILIZATION IN MULTI-LEVEL, MULTI-LINE COMMUNICATION SYSTEMS"	Examiner Name: Unknown
	Attorney Docket No.: RA-194

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A						RECEIVED SEP 03 2003 Technology Center 2600
	B						
	C						
	D						
	E						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	F							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>E/B</i>	G	Raghavan, S.A. et al. "Nonuniformly Spaced Tapped-Delay-Line Equalizers," IEEE Transactions on Communications, Vol. 41, No. 9, September 1993, pp 1290-1295.
<i>9</i>	H	Ariyavisitakul, Sirikiat et al. "Reduced-Complexity Equalization Techniques for Broadband Wireless Channels," IEEE Journal on Selected Areas in Communications, Vol. 15, No. 1, January 1997, pp 5-15.
<i>4</i>	I	Sidiropoulos, Stefanos et al. "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers," IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690.
<i>F'</i>	J	

Examiner

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.